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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,350	11/09/2001	Suk-Kyun Lee	29347/597	1665

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EXAMINER	
NGUYEN, DAO H	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 03/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/045,350	LEE, SUK-KYUN	
	Examiner	Art Unit	
	Dao H Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the communications dated 12/29/2003, claims 1-9 are active in this application as a result of the cancellation of claims 10-17.

Remarks

2. Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 U.S.C. § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim(s) 1-9 is/are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 5,751,054 to Yilmaz et al., in view of Imoto, U.S. Patent No. 5,920,781.

Regarding claim 1, Yilmaz discloses a semiconductor element, as shown in figures 16, 23, comprising:

a p-substrate 10,

a first DMOS element (20V DMOS – fig. 16a, or 234 – fig. 23) formed on a first portion A of the substrate 10; and

a first MOS element (16V NMOS) formed on a second portion E of the substrate that is separate from the first portion A.

Yilmaz does not teach that the DMOS element includes a gate electrode having slanted side walls.

Imoto discloses a DMOS device, as shown in figures 1(A-D), including a gate electrode 13 having slanted side walls 15, 16.

It would have been obvious to one of ordinary skills in the art at the time the invention was made to modify the invention of Yilmaz so that it would have a slanted-side-walls gate electrode as that of Imoto in order for the ion-implanted impurities be able to penetrate the gate electrode more easily through its side parts to increase the channel length of channel regions, therefore to increase the characteristics of the device. See column 3, lines 9-21, and column 6, lines 2-9 of Imoto.

Regarding claim 2, Yilmaz/Imoto disclose the semiconductor element wherein the slanted side walls of the gate electrode of the first DMOS element and side walls of a gate electrode of the first MOS element have different profiles. See figures 16 of Yilmaz and figures 1 of Imoto.

Regarding claim 3, Yilmaz/Imoto disclose the semiconductor element wherein the first DMOS element includes:

a well 40 of a first conductive type (N-type) formed on the substrate 10;

a body region 239 of a second conductive type (P-type) formed in the well 40;

a source region 243 of the first conductive type (N-type) formed in the body region 239;

a drain region (242) of the first conductive type (N-type) formed in the well 40 and spaced from the source region 243; and

a gate insulating layer 232/245 formed between the well 40 and the gate electrode 248. See figures 23, and column 17, line 1 to column 18, line 38.

Regarding claim 4, Yilmaz/Imoto disclose the semiconductor element wherein a portion of one of the slanted side walls overlaps a part of the source region. See figure 23 of Yilmaz, and figures 1 of Imoto.

Regarding claim 5, Yilmaz/Imoto disclose the semiconductor element wherein the first MOS element includes:

a well (P-well) of a first conductive type (P-type) formed on the substrate (P-substrate);

a source region 153 of a second conductive type (N-type) formed in the well;

a drain region 154 of the second conductive type (N-type) formed in the well;

a gate electrode formed on the well of the first conductive type; and

a gate insulating layer interposed between the gate electrode and the well of the first conductive type. See figures 15-16 of Yilmaz.

Regarding claim 6, Yilmaz/Imoto disclose the semiconductor element wherein a gate insulating layer 232/245 of the first DMOS 234 element includes a relatively thicker portion 245. See figure 23 of Yilmaz.

Regarding claim 7, Yilmaz/Imoto disclose the semiconductor element comprising all claimed limitations. See figures 23 of Yilmaz. Furthermore, it is well known in the art that every MOS device should have such protection layer as claimed in order to protect the device from external effect(s), and that contacts must be made to the source/drain region of the device to input/output signal in/out of the device.

Regarding claims 8-9, Yilmaz/Imoto disclose the semiconductor element comprising all claimed limitations. This is inherent and well known in the art since multiple identical semiconductor devices being made in the same semiconductor element/package would increase the performance of the package and further would decrease the cost of the product.

Conclusion

5. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax numbers for all communication(s) is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Dao H. Nguyen
Art Unit 2818
March 01, 2004